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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/798,227	02/11/97	KEETH B	660073.587

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EXAMINER	
RANSOM, D	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/798,227	Applicant(s) Keeth
	Examiner David Ransom	Group Art Unit 2752

☒ Responsive to communication(s) filed on *Feb 11, 1997*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-15* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-15* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *AR-AT*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

The writing in the drawings are faint and will not reproduce well. Drawings 1, 3 and 5 do not conform to the paper standards acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1 through 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent Number 5,577,236}.

For claims 1 to 5 Johnson provides a method of adjusting data timing in a memory subsystem (column 6 lines 19 to 46), a memory device (column 5 lines 34 to 47), a memory module controller (column 5 line 48 through column 6 line 18), initial output timing at the memory device (column 7 lines 21 to 40), transmitting a first set of data from the memory device to the memory controller according to timing (column 5 lines 19 to 33), echo clock signal

transmission from memory device to memory controller (column 6 line 47 through column 7 line 3), the memory controller receiving the echo clock signal (column 6 lines 19 to 46), echo clock signal phase error relative to the master clock signal identification (column 6 lines 19 to 46), initial output revising in response to phase error (column 6 lines 19 to 46), transmitting a second set of data from the memory device to the memory controller according to the revised output timing (column 6 lines 19 to 46), Identification of phase error of the received echo clock signal relative to the master clock signal (column 6 lines 8 to 18), generating a plurality of phased shifted signals responsive to the master clock signal (column 6 lines 8 to 18), comparing the echo clock signal to each of the phased echo clock signals (column 6 lines 8 to 18), identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal (column 6 lines 8 to 18), setting a delay of delay circuit (column 6 line 47 through column 7 line 3), applying the master clock signal to the delay circuit to produce the echo clock signal (column 6 line 47 through column 7 line 3), storing data in an output register (column 6 line 47 through column 7 line 3), clocking the register with the echo clock signal (column 6 line 47 through column 7 line 3), outputting data from the register in response to the echo clock signal (column 6 line 47 through column 7 line 3), the step of establishing an initial output timing includes the step of adjusting the delay of the delay circuit (column 5 line 48 through column 6 line 17).

4. Claims 6, 8 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent Number 5,577,236}.

For claims 6, 8 and 9 Johnson provides a master clock signal generation (column 5 line 48 through column 6 line 18), master clock signal transmission from the memory controller to memory device (column 5 line 48 through column 6 line 18), first read command issued to memory device (column 5 line 48 through column 6 line 18), first data set read from the memory device in response to read command (column 5 line 48 through column 6 line 18), producing an echo signal at the memory device in response to the first read command (column 5 line 48 through column 6 line 18), the echo signal has a phase shift relative to the master clock signal (column 6 lines 19 to 46), transmission of an echo signal to the memory controller (column 5 line 48 through column 6 line 18), receiving an echo signal at the memory controller (column 6 lines 19 to 46), comparing the echo signal to the master clock signal (column 6 lines 8 to 18), selecting an adjusted time delay in response to the step of comparing the echo signal to the master clock signal (column 7 lines 21 to 40), issuing a second read command to the memory device (column 5 line 48 through column 6 line 18), reading a second set of data in response to the second read command (column 5 line 48 through column 6 line 18), second data set transmission to the memory controller with adjusted time delay (column 5 line 48 through column 6 line 18), generating a plurality of phased shifted signals responsive to the master clock signal (column 6 lines 8 to 18), comparing the echo signal to each of the phase shifted signals (column 6 lines 8 to 18), phased signal identification that is closest to the echo clock signal (column 7 lines 21 to 40).

5. Claims 10 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent Number 5,577,236}.

For claims 10 and 11 Johnson provides a memory controller for a memory system with a plurality of memory devices coupled to a common clock and command bus (column 5 line 48 through column 6 line 8), the memory devices producing echo signals in response to clock signals on the clock bus (column 6 lines 19 to 46), the controller with a clock source coupled to the clock bus operative to produce a master clock signal (column 6 lines 19 to 46), a phase comparing circuit coupled to the clock bus (column 7 lines 21 to 40), a logic circuit coupled to the phase comparing circuit and adapted to produce adjustment data in response to the phase signal (column 6 lines 8 to 18), a control data circuit having a command output coupled to the command bus (column 5 line 48 through column 6 line 18), the command output produces a command signal in response to the adjusted data (column 6 lines 8 to 18), a signal source having a plurality of outputs and operative to produce a plurality of phase shifted signal at the outputs in response to the master clock signals (column 6 lines 19 to 46), a plurality of phase comparator (column 7 lines 21 to 40), each phase comparator includes a first input coupled to a signal source outputs (column 7 lines 21 to 40), a second input coupled to the clock bus and a phase output coupled to the logic circuit (column 7 lines 21 to 40).

6. Claims 13, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent Number 5,577,236}.

For claims 13, 14 and 15 Johnson provides a memory system (figure 3), a command bus (figure 3 item 349), a clock bus (figure 3 item 348), a data bus (figure 3 items 305 and 311), a memory controller with a master clock generator (figure 3 item 302), a master clock generator

coupled with the clock bus (figure 3 item 303), a phase comparator with a first input coupled to the master clock generator (figure 3 item 319), a phase comparator with a second input (figure 3 item 318), a phase comparator with responsive with the phase difference between two inputs to produce an adjust command (figure 3 items 318, 319 and 322), a logic circuit (figure 3 item "to logic circuitry"), a memory device having a clock input coupled to the clock bus (figure 3 item 349), an echo signal generator responsive to the master clock signal at the clock input (figure 3 items 304 and 314), the echo signal generator being coupled to the second input of the phase comparator (figure 3 item 313 and 319), a data latch with a trigger input and responsive to a control signal at the trigger's input to transmit data to the data bus (figure 3 item 322), a variable delay circuit having a control output coupled to the trigger input and a command input coupled to the command bus (figure 3 item 306), the delay circuit being responsive to the adjust command on the command bus to produce a delay corresponding to the adjust command (figure 3 items 306 to 311), a signal source having a plurality of outputs (figure 3 items 304 and 350), outputs operate to produce a plurality of phase shifted signals at the outputs in response to the master clock signal (figure 3 items 304 and 350), a plurality of phase comparator (figure 3 items 318 and 319), a first comparator input coupled to signal source input (figure 3 item 319), a second input coupled to the clock bus and a phase output coupled to the logic circuit (figure 3 item 318), the signal source includes multiple output delay locked loop (figure 3 item 313).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US Patent Number 5,577,236} as applied to claim 6 above, and further in view of Smith {US Patent Number 5,020,023}.

Johnson discloses the invention substantially as claimed. Johnson provides the elements as in claim 6 as stated above. However, Johnson does not disclose a time delay including adjusting a vernier. Smith teaches the use of a vernier to allow in a sender and receiver system for near synchronous operation. For claim 7 Smith provides a time delay includes adjusting a vernier (abstract or column 3 line 35 through column 4 line 30). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a vernier in order to increase the accuracy of a serial input array as is stated in Johnson for the capturing of clock signals from the network. It will therefor fulfill the requirement of receiver and comparator for the claimed invention in Johnson. A operator, may wish to upgrade the one or series of independent latches in Johnson and replace it with a preexisting machine that links the data from the latches to create a signal to identify the phase difference. The detectors given appear to be generic detectors.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US Patent Number 5,577,236} as applied to claim 6 above, and further in view of Jeddeloh et al. {US Patent Number 5,692,165}.

Johnson discloses the invention substantially as claimed. Johnson provides the elements in claims 10 and 11 as stated above. However, Johnson does not disclose a signal source including a multiple output delay locked loop (column 6 lines 19 to 46). Jeddeloh teaches the use of a delay locked loop in an electronic device such as a memory device for the purpose of solving the problem of time skew. For claim 12 Jeddeloh provides a signal source including a multiple output delay locked loop (column 1 lines 31 to 45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a delay lock loop in place of the delay module in order to provide a more up to date component, superior performance or less cost. The use of a delay locked loop would provide the user with similar operation to the delay module as listed in Johnson. In the interest of providing cross platform compatibility and maximizing resources, the repairman may wish to utilize a more up to date phase locked loop over the provided delay module because of features of improvement that will not normally require a patent (raw performance upgrades or cost).

Johnson creates a clock selector to limit the clock signals that are sent to the delay modules allowing one phase to be read at one time. Parallel delay modules allow for immediate comparison and more accurate comparisons, baring the overloading of the echo clock bus. Five delay modules should not face this problem.

Conclusion

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or faxed to: (730)308-9051 (for formal communications intended for entry) or (703)308-9051 (for informal or draft communications, please label "PROPOSED" or "DRAFT"); Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA 22209, sixth floor receptionist.

Any inquiry concerning this communication should be directed to David Ransom at telephone number (703) 305-4035. The examiner can normally be reached on Monday through Friday from 9:00 to 5:00. If there is any problem contacting me call Tod Swann at (703)308-7791. The fax number to this office (branch 2318) is (703)308-5357.

Any inquiry of a general nature or relating to the status of this applications or proceeding should be directed to the group receptionist whose telephone number is (703)305-3900.

David Ransom
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